It very important to measure the capacitance difference for integrated circuits as some silicon structures are very sensitive to noise , acceleration and pressure as well as vibrations.

**The following methods are used to measure the capacitance -**  
 Use oscillator to drive the capacitance bridge circuit.It is the change which is relative to reference capacitance.It produces the output voltage or shift in frequency. For some we can not use parasitic capacitance as a readout circuit as it can cause error in measurement. For time being a innovative switched capacitor techniques is used but it is inherent to all switched- capacitor circuit. Also MOS switch charge injection , clock feedthrough and circuit noise are the major factors affecting on circuit performance. So given paper is all about the digital technique for measuring capacitance difference.It has its origins in charge redistribution A/D converters, op-amp offset or charge injection problems.  
  
In 1979 , one algorithm was developed, that calculate the ratio errors from sequence of measurement based on charge redistribution and it was implemented to find the capacitor mismatched error which cause linearity errors in charge redistribution A/D converters. Also MOS switch charge injection was ignored due to large size of capacitor. Also it is very crucial to eliminate charge injection sources to get higher resolutions and smaller errors in A/D converters. This higher resolution and elimination of errors can be achieved by self- calibration technique which is caused by charge injection and component mismatched, also it can be used to measure capacitance differences and random source of charge injection. MOS charged injection must be canceled as it caused large errors.so the give technique in paper is compensate with errors due to capacitive mismatched, comparator offset and charge injection.  
**The circuit diagram is explain below:  
  
Conclusion:**  
The technique is given in this paper can measure capacitance differences with a resolution of 0.05 fF on capacitor in the 20 - 100fF range in the presence of parasitic capacitance which is almost 100 times larger.also charge injection,parasitic capacitance , voltage and temperature coefficients which are nonideal can be negligible or can be calibrated.also capacitor hysteresis , junction leakage and threshold voltage are shown as very small so it is ignored. This digital averaging is increases resolution with increases measurement time. Charge redistribution technique can be directly applied to sensor as it measure the capacitance difference and it is very simple as it requires three capacitors, a voltage comparator, successive approximation register (SAR) and a D/A converter, also it provides inherent readout and high resolution. This is compatible with digital signal processing and ideally suited fot readout in capacitance difference measuresment.